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| **Subject: Digital Electronics**  **Name of the Faculty: Revti Raman (CSE-3rd)** | | | | | | | |
| Week | Topic(Theory) | | | | | **Topic(Practical)** | |
| 1 | Distinction between analog and digital signal. Applications and advantages of digital signals | | | | | Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates | |
| 2 | Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary and vice-versa.  Binary addition and subtraction including binary points. 1’s and 2’s complement method of addition/subtraction | | | | |
| 3 | Concept of code, weighted and non-weighted codes, examples of 8421, BCD, excess-3 and Gray code.  Concept of parity, single and double parity and error detection | | | | |
| 4 | Concept of negative and positive logic  Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR, EXOR Gates, NAND and NOR as universal  gates. | | | | |
| 5 | Introduction to TTL and CMOS logic families  Postulates of Boolean algebra, De Morgan’s Theorems. Implementation of Boolean (logic) equation with gates | | | | | Realisation of logic functions with the help of NAND or NOR gates | |
| 6 | Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits | | | | | To design a half adder using XOR and NAND gates and verification of its operation  Construction of a full adder circuit using  XOR and NAND gates and verify its operation | |
| 7 | Half adder and implementation.  4 bit adder circuit | Full | adder | circuit, design | and | Verification of truth table for encoder and decoder ICs, Mux and DeMux | |
| 8 | Four bit decoder circuits for 7 segment display and decoder/driver ICs.  Basic functions and block diagram of MUX and DEMUX with different ICs  Basic functions and block diagram of Encoder | | | | |
| 9 | Concept and types of latch with their working and applications  Operation using waveforms and truth tables of RS, T, D, Master/Slave JK flip flops.  Difference between a latch and a flip flop | | | | |
| 10 | Introduction to Asynchronous and Synchronous counters Binary counters | | | | | Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-  flops). | |
| 11 | Divide by N ripple counters, Decade counter, Ring counter | | | | | To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation | |
| 12 | Serial in parallel out, serial in serial out, parallel in serial out | | | | |
| 13 | parallel in parallel out.Universal shift register | | | | |
| 14 | Working principle of A/D and D/A converters  Brief idea about different techniques of A/D conversion and | | | | |
|  | study of :Stair step Ramp A/D converterDual Slope A/D converterSuccessive Approximation A/D Converter | | | | | |  |
| 15 | Detail study of : Binary Weighted D/A converterR/2R ladder D/A converter Applications of A/D and D/A converter | | | | | |  |
| **6** | Memory organization, classification of semiconductor memories (RAM, ROM, PROM, EPROM, EEPROM),  static and dynamic RAM, introduction to 74181 ALU IC | | | | | | To design a 4 bit ring counter and verify its operation.  Use of Asynchronous Counter ICs (7490 or 7493) |

Note: Last (5th) Lecture of week will be the revision lecture. Practical/Lab. Experiments will be conducted as per the latest guidelines of Higher Authority.